AMENDMENTS TO THE CLAIMS:

The listing of claims below will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method comprising:

receiving a sequence of symbols modulated onto a carrier frequency over a channel;

demodulating the symbols using a clock frequency;

determining a frequency offset of the received symbols with respect to the clock frequency;

integrating the frequency offset over a predetermined number of symbols to create an integrator signal; and

applying the ~~determined frequency offset~~integrator signal to adjust the clock frequency.

2. (Canceled).

3. (Currently Amended) The method of claim [[2]]1 wherein the predetermined number of symbols is sufficient to compensate for short term variations in the clock frequency.

4. (Currently Amended) The method of claim 1, further comprising analyzing the received symbols for a sequence that identifies ~~the~~a source of the sequence and enabling or disabling the application of the frequency offset to adjust the clock frequency based on the source of the symbols.

5. (Currently Amended) The method of claim 1 wherein ~~adjusting the clock frequency~~ applying the integrator signal comprises applying a voltage to a voltage controlled oscillator.

6. (Original) The method of claim 1 wherein determining a frequency offset comprises determining a frequency offset with respect to the carrier frequency.

7. (Original) The method of claim 1 wherein the sequence of symbols is modulated onto the carrier frequency using phase shift keying and wherein determining a frequency offset comprises determining a phase rotation of the phase shift keyed symbols.

8. (Original) The method of claim 1 further comprising applying the adjusted clock frequency to transmit a sequence of symbols modulated on a carrier frequency.

9. (Original) The method of claim 8 wherein the adjusted clock frequency is applied to the transmission rate of the symbol sequence and to the carrier frequency.

10. (Original) The method of claim 1 wherein the adjusted clock frequency is a master clock frequency for a terminal.

11. (Currently Amended) An apparatus comprising:

a receiver to receive a sequence of symbols modulated on a carrier frequency;

an adjustable clock to generate a clock frequency for use in receiving and transmitting;

a demodulator to demodulate the received symbols and to determine a frequency offset of the received symbols with respect to the clock frequency; and

an adjustment drive circuit to receive the frequency offset and generate a clock adjustment signal for application to the adjustable clock, the adjustment drive circuit including a short term integrator to integrate the frequency offset over a predetermined number of symbols.

12. (Canceled).

13. (Currently Amended) The apparatus of claim [[12]]13 wherein the predetermined number of symbols is sufficient to compensate for short term variations in the clock frequency.

14. (Currently Amended) The apparatus of claim 11 further comprising a deframer to analyze the received symbols for a sequence that identifies ~~the~~a source of the

sequence and a switch coupled to the deframer to enable or disable the application of a frequency offset to adjust the clock frequency based on the source of the symbols.

15. (Original) The apparatus of claim 11 wherein the adjustable clock comprises a voltage controlled oscillator and wherein the adjustment drive circuit comprises a digital to analog converter to generate an adjustment voltage to apply to the voltage controlled oscillator.

16. (Original) The apparatus of claim 11 wherein the frequency offset comprises a frequency offset with respect to the carrier frequency.

17. (Original) The apparatus of claim 11 wherein the received symbols are modulated onto the carrier frequency using phase shift keying and wherein the frequency offset comprises a phase rotation of the phase shift keyed symbols.

18. (Original) The apparatus of claim 11 further comprising a modulator to modulate a sequence of symbols on a carrier frequency using the adjusted clock frequency.

19. (Original) The apparatus of claim 18 wherein the adjusted clock frequency is applied to the transmission rate of the symbol sequence and to the carrier frequency.

20. (Original) The apparatus of claim 11 wherein the adjustable clock comprises a master clock for the apparatus.

21. (Currently Amended) A machine-readable medium having stored thereon data representing instructions which, when executed by a machine, cause the machine to perform operations comprising:

receiving a sequence of symbols modulated onto a carrier frequency over a channel;

demodulating the symbols using a clock frequency;

determining a frequency offset of the received symbols with respect to the clock frequency;

integrating the frequency offset over a predetermined number of symbols to create an integrator signal; and

applying the ~~determined frequency offset~~integrator signal to adjust the clock frequency.

22. (Canceled).

23. (Original) The medium of claim [[22]]21 wherein the predetermined number of symbols is sufficient to compensate for short term variations in the clock frequency.